



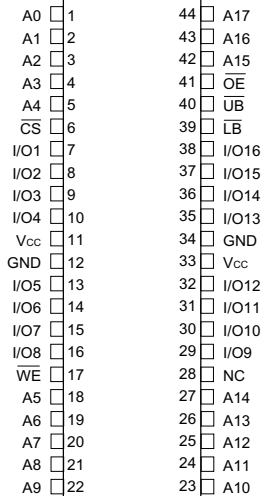
256Kx16 MONOLITHIC SRAM, SMD 5962-96902

FEATURES

- Access Times 17, 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
 - 44 pin Ceramic SOJ (Package 102)
 - 44 lead Ceramic Flatpack (Package 225)
 - 44 lead Formed Ceramic Flatpack
- Organized as 256Kx16
- Data Byte Control:
 - Lower Byte (\overline{LB}) = I/O₁₋₈
 - Upper Byte (\overline{UB}) = I/O₉₋₁₆
- 2V Minimum Data Retention for battery back up operation (WMS256K16L-XXX Low Power Version Only)
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

PIN CONFIGURATION FOR WMS256K16-XXX

44 CSOJ
44 FLATPACK
TOP VIEW



PIN DESCRIPTION

A ₀₋₁₇	Address Inputs
\overline{LB}	Lower-Byte Control (I/O ₁₋₈)
\overline{UB}	Upper-Byte Control (I/O ₉₋₁₆)
I/O ₁₋₁₆	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V _{cc}	+5.0V Power
GND	Ground
NC	No Connection



TRUTH TABLE

CS	WE	OE	LB	UB	Mode	Data I/O		Power
						I/O1-8	I/O9-16	
H	X	X	X	X	Not Select	High Z	High Z	Standby
L	H	H	X	X	Output Disable	High Z	High Z	Active
L	X	X	H	H				
L	H	L	L	H	Read	Data Out	High Z	Active
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	Active
			H	L		High Z	Data In	
			L	L		Data In	Data In	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	TA	-55	+125	°C
Storage Temperature	TSTG	-65	+150	°C
Signal Voltage Relative to GND	VG	-0.5	VCC+0.5	V
Junction Temperature	TJ		150	°C
Supply Voltage	VCC	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC	4.5	5.5	V
Input High Voltage	VIH	2.2	VCC + 0.3	V
Input Low Voltage	VIL	-0.3	+0.8	V
Operating Temp. (Mil.)	TA	-55	+125	°C

CAPACITANCE
(TA = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	CIN	VIN = 0V, f = 1.0MHz	20	pF
Output capacitance	COU	VOU = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Sym	Conditions	Units		
			Min	Max	
Input Leakage Current	ILI	VCC = 5.5, VIN = GND to VCC		10	µA
Output Leakage Current	ILO	CS = VIH, OE = VIH, VOUT = GND to VCC		10	µA
Operating Supply Current	ICC	CS = VIL, OE = VIH, f = 5MHz, VCC = 5.5		275	mA
Standby Current	ISB	CS = VIH, OE = VIH, f = 5MHz, VCC = 5.5		17	mA
Output Low Voltage	VOL	IOL = 8mA, VCC = 4.5		0.4	V
Output High Voltage	VOH	IOH = -4.0mA, VCC = 4.5	2.4		V

NOTE: DC test conditions: VIH = VCC - 0.3V, VIL = 0.3V

LOW POWER DATA RETENTION CHARACTERISTICS (WMS256K16L-XXX ONLY)
(TA = -55°C TO +125°C)

Parameter	Symbol	Conditions	Units			
			Min	Typ	Max	
Data Retention Supply Voltage	VDR	CS ≥ VCC - 0.2V	2.0		5.5	V
Data Retention Current	ICCDR1	VCC = 3V		1.0	8.0	mA



AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	t _{RC}	17		20		25		35		ns
Address Access Time	t _{AA}		17		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25		35	ns
Output Enable to Output Valid	t _{OE}		10		12		15		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	2		5		5		5		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		9		10		12		15	ns
Output Disable to Output in High Z	t _{OHZ} ¹		9		10		12		15	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	t _{BA}		10		12		14		17	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Enable to Low Z Output	t _{BLZ} ¹	0		0		0		0		ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Disable to High Z Output	t _{BHZ} ¹		9		10		12		15	ns

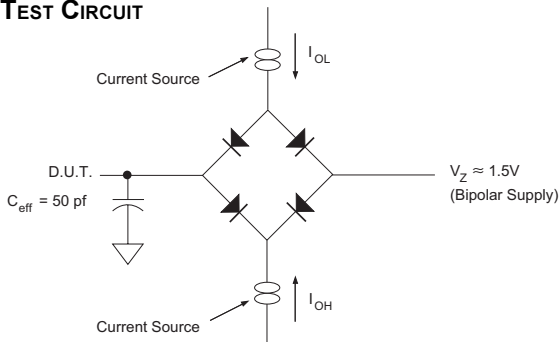
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	-17		-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t _{WC}	17		20		25		35		ns
Chip Select to End of Write	t _{CW}	14		17		20		25		ns
Address Valid to End of Write	t _{AW}	14		17		20		25		ns
Data Valid to End of Write	t _{DW}	10		12		15		20		ns
Write Pulse Width	t _{WP}	14		17		20		25		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	2		2		2		2		ns
Output Active from End of Write	t _{OW} ¹	0		0		0		0		ns
Write Enable to Output in High Z	t _{WHZ} ¹		9		10		10		15	ns
Data Hold Time	t _{DH}	0		0		0		0		ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Valid to End of Write	t _{BW}	14		17		20		25		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

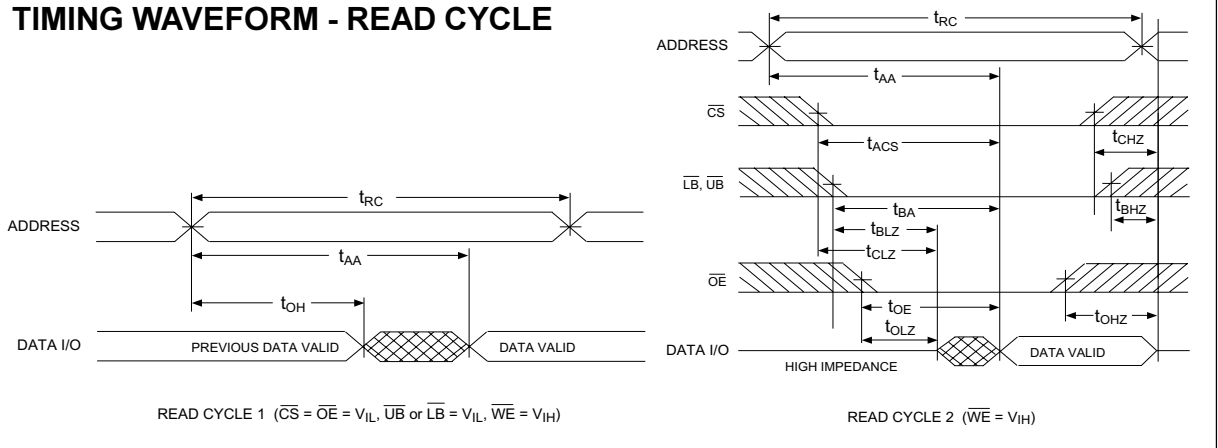
Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

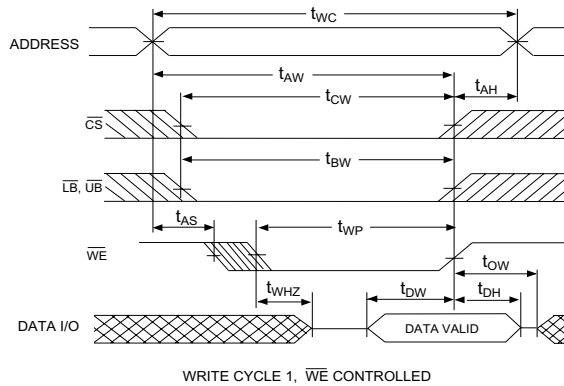
- V_Z is programmable from -2V to +7V.
- I_{OL} & I_{OH} programmable from 0 to 16mA.
- Tester Impedance Z₀ = 75 Ω.
- V_Z is typically the midpoint of V_{OH} and V_{OL}.
- I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.



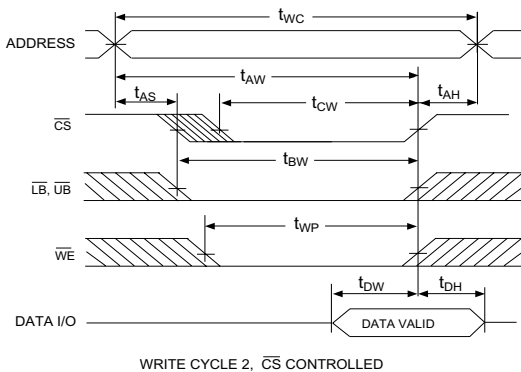
TIMING WAVEFORM - READ CYCLE



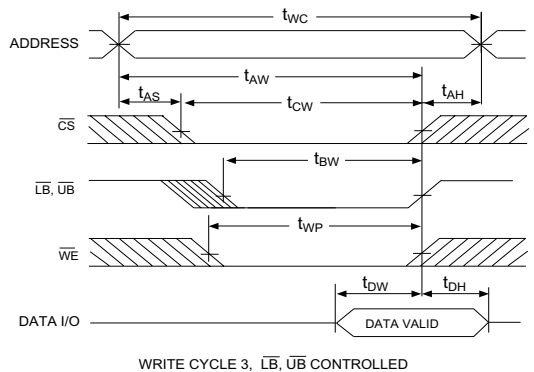
WRITE CYCLE - WE CONTROLLED



WRITE CYCLE - CS CONTROLLED

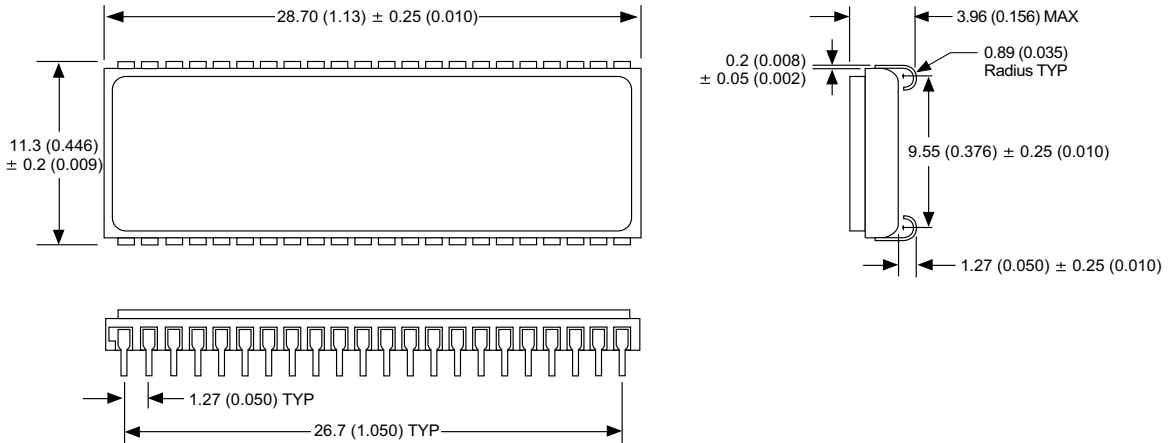


WRITE CYCLE - LB, UB CONTROLLED



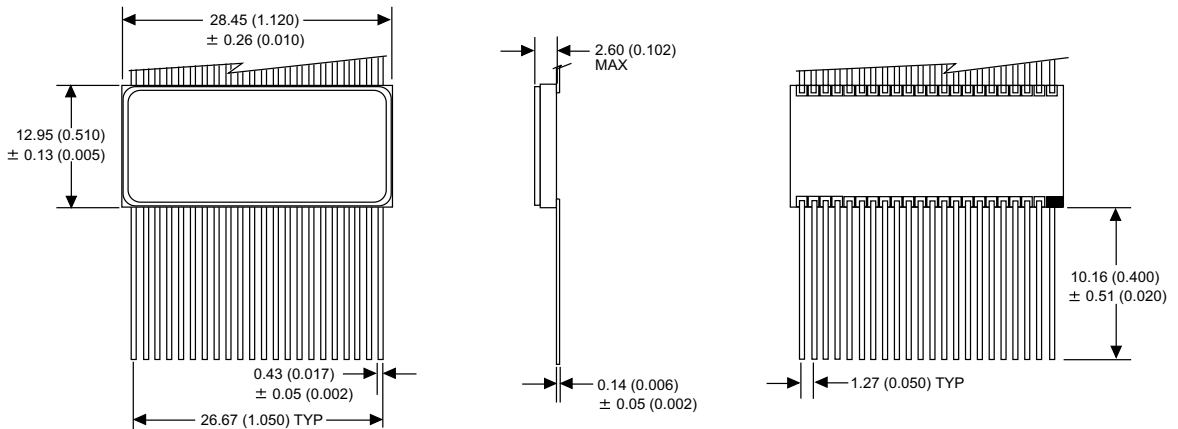


PACKAGE 102: 44 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

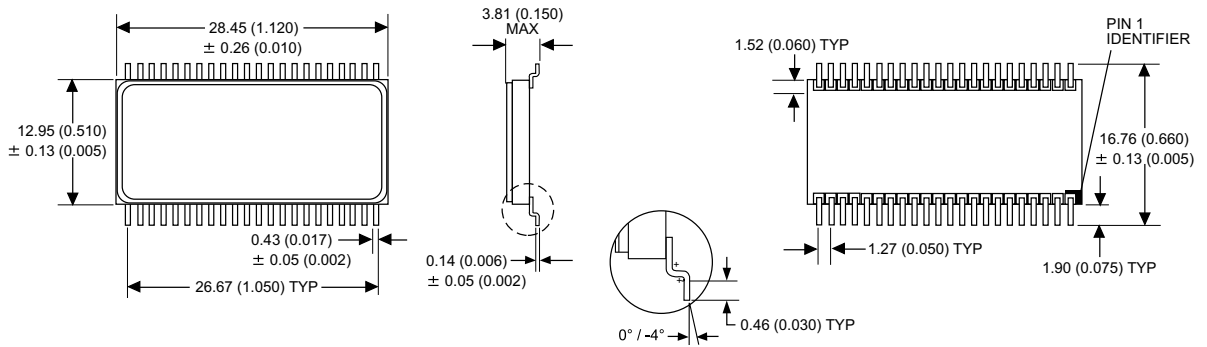
PACKAGE 225: 44 LEAD, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 211: 44 LEAD FORMED, CERAMIC FLAT PACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M S 256K16 X - XXX X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- DL = 44 Lead Ceramic SOJ (Package 102)
- FL = 44 Lead Ceramic Flatpack (Package 225)
- FG = 44 Lead Formed Ceramic Flatpack

ACCESS TIME (ns)

IMPROVEMENT MARK:

- Blank = Standard Power
- L = Low Power Data Retention

ORGANIZATION, 256K x 16

SRAM

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
256K x 16 SRAM Monolithic	35ns	44 lead SOJ (DL)	5962-96902 01HMX
256K x 16 SRAM Monolithic	25ns	44 lead SOJ (DL)	5962-96902 02HMX
256K x 16 SRAM Monolithic	20ns	44 lead SOJ (DL)	5962-96902 03HMX
256K x 16 SRAM Monolithic	17ns	44 lead SOJ (DL)	5962-96902 04HMX
256K x 16 SRAM Monolithic	35ns	44 lead Flatpack (FL)	5962-96902 01HNX
256K x 16 SRAM Monolithic	25ns	44 lead Flatpack (FL)	5962-96902 02HNX
256K x 16 SRAM Monolithic	20ns	44 lead Flatpack (FL)	5962-96902 03HNX
256K x 16 SRAM Monolithic	17ns	44 lead Flatpack (FL)	5962-96902 04HNX
256K x 16 SRAM Monolithic	35ns	44 lead Formed Flatpack (FG)	5962-96902 01HTX
256K x 16 SRAM Monolithic	25ns	44 lead Formed Flatpack (FG)	5962-96902 02HTX
256K x 16 SRAM Monolithic	20ns	44 lead Formed Flatpack (FG)	5962-96902 03HTX
256K x 16 SRAM Monolithic	17ns	44 lead Formed Flatpack (FG)	5962-96902 04HTX